PATENT ABSTRACTS OF JAPAN

(11)Publication number : **06-084692**
(43)Date of publication of application : **25.03.1994**

(51)Int.CI. **H01G 4/12**
C04B 35/46
C04B 35/64
H01B 3/12

(21)Application number : **05-085705**
(22)Date of filing : **19.03.1993**

(71)Applicant : **TDK CORP**
(72)Inventor : **NAKANO YUKIE**
ARASHI TOMOHIRO
SATO AKIRA
NOMURA TAKESHI

(30)Priority
Priority number : **04208483** Priority date : **13.07.1992** Priority country : **JP**

(54) MULTILAYER CERAMIC CHIP CAPACITOR

(57)Abstract:
PURPOSE: To realize a multilayer ceramic chip capacitor which can satisfy both temperature characteristics of capacity, i.e., X7R characteristics (EIA regulation) and B characteristics (EIAJ regulation), and in which aging of capacity is slow under DC field and acceleration lifetime of insulation resistance IR is long.
CONSTITUTION: The multilayer ceramic chip capacitor employs a dielectric layer having composition of MgO: 0.1-3mol., MnO: 0.05-1.0-mol., Y2O3: 1mol. or less, BaO+CaO: 2-12mol.(including BaO or CaO=0), and SiO2: 2-12mol. for 100mol. of BaTiO3.

LEGAL STATUS

[Date of request for examination]	11.01.1996
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	2762427
[Date of registration]	27.03.1998
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1] It is the laminating type ceramic chip capacitor which has the capacitor chip object of composition of that the laminating of a dielectric layer and the internal-electrode layer was carried out by turns. the aforementioned dielectric layer a barium titanate as an accessory constituent as a principal component A magnesium oxide, Manganese oxide and at least one sort chosen from a barium oxide and a calcium oxide, Silicon oxide is contained and it is a barium titanate BaTiO3 A magnesium oxide to MgO manganese oxide -- MnO -- a barium oxide -- BaO -- a calcium oxide -- CaO -- silicon oxide -- SiO2 When it converts, respectively The ratio to BaTiO3 100 mol is MgO:0.1-3 mol, MnO:0.05-1.0 mol, BaO+CaO:2-12 mol, and SiO2. : Laminating type ceramic chip capacitor characterized by being 2-12 mols.

[Claim 2] It is BaO, CaO, and SiO2 to the above BaTiO3 and the sum total of MgO and MnO. Laminating type ceramic chip capacitor of the claim 1 contained one to 10% of the weight as y (Bax calcium1-x O) and SiO2 (however, it is 0.3<=x<=0.7 and 0.95<=y<=1.05.).

[Claim 3] It is the laminating type ceramic chip capacitor which has the capacitor chip object of composition of that the laminating of a dielectric layer and the internal-electrode layer was carried out by turns. the aforementioned dielectric layer a barium titanate as an accessory constituent as a principal component A magnesium oxide, Manganese oxide, a yttrium oxide, and at least one sort chosen from a barium oxide and a calcium oxide, Silicon oxide is contained and it is a barium titanate BaTiO3 A magnesium oxide to MgO To MnO, it is a yttrium oxide about manganese oxide Y2 O3 In BaO, it is [barium oxide] silicon oxide to CaO about a calcium oxide SiO2 When it converts, respectively, The ratio to BaTiO3 100 mol is MgO:0.1-3 mol, MnO:0.05-1.0 mol, and Y2 O3. : One mol or less, BaO+CaO:2-12 mol, SiO2 : Laminating type ceramic chip capacitor characterized by being 2-12 mols.

[Claim 4] BaTiO3, MgO, MnO, and Y2 O3 It is BaO, CaO, and SiO2 to the sum total. Laminating type ceramic chip capacitor of the claim 3 contained one to 10% of the weight as y (Bax calcium1-x O) and SiO2 (however, it is 0.3<=x<=0.7 and 0.95<=y<=1.05.).

[Claim 5] The claim 1 whose electric conduction material contained in the aforementioned internal-electrode layer is nickel or nickel alloy, or one laminating type ceramic chip capacitor of 4.

[Claim 6] Oxygen tension is 10-8 to 10-12. Laminating type ceramic chip capacitor of the claim 5 calcinated within the 1200-1400-degree C temperature requirement in the atmosphere which is atmospheric pressure.

[Claim 7] The laminating type ceramic chip capacitor of the claims 5 or 6 which annealed oxygen tension within the temperature requirement 1100 degrees C or less in the atmosphere of 10 to 6 or more atmospheric pressure after baking.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to a laminating type ceramic chip capacitor.
[0002]
[Description of the Prior Art] The laminating type ceramic chip capacitor is widely used as small, large capacity, and highly reliable electronic parts, and the number used in one set of electronic equipment also reaches a large number. In recent years, the demand to small [to a laminating type ceramic chip capacitor / further], large capacity, a low price, and high-reliability-izing is still severer with small and highly-efficient-izing of a device.
[0003] Usually, a laminating type ceramic chip capacitor carries out the laminating of the paste for internal-electrode layers, and the paste for dielectric layers by the sheet method, print processes, etc., they really carry out simultaneous baking, and it is manufactured.
[0004] Although Pd and Pd alloy are generally used for the electric conduction material of an internal-electrode layer, since Pd is expensive, base metal, such as comparatively cheap nickel and nickel alloy, is being used. In order for an internal-electrode layer to oxidize if it calcinates in the atmosphere when using base metal as electric conduction material of an internal-electrode layer, it is necessary to perform simultaneous baking with a dielectric layer and an internal-electrode layer in a reducing atmosphere. However, if it calcinates in a reducing atmosphere, since a dielectric layer will be returned and specific resistance will become low, nonreducible dielectric materials are proposed.
[0005] However, the life of insulation resistance IR becomes short and the laminating type ceramic chip capacitor using nonreducible dielectric materials has a problem of a low in reliability.
[0006] Moreover, if a dielectric is exposed to direct-current electric field, it is specific-inductive-capacity epsilons. The problem of falling with time arises. If thickness of a dielectric layer is made thin for a chip capacitor in order to large-capacity-ize, small and, since the electric field concerning the dielectric layer when impressing direct current voltage will become strong, it is specific-inductive-capacity epsilons. Aging, i.e., aging of capacity, will become remarkably large.
[0007] By the way, by the specification called X7R property set to the EIA standard, the rate of change of capacity is determined as less than (25 degrees C of reference temperature) **15% from -55 to 125 degrees C.
[0008] As dielectric materials which satisfy X7R property, the composition of a BaTiO3+SrTiO3+MnO system shown, for example in JP,61-36170,A is known. However, aging of the capacity under direct-current electric field is large, for example, this thing is 50V at 40 degrees C. When direct-current electric field are impressed for 1000 hours, the rate of change of capacity becomes about -10--30%, and it becomes impossible to satisfy X7R property.
[0009] moreover, in addition to this as a nonreducible dielectric porcelain constituent BaTiO3+MnO+MgO currently indicated by JP,57-71866,A, a Ti1-y Zry O2+alpha(1-z) (MnO+zCoO)+beta(1-t) (A2 O5+tL 2O3)+wSiO2 (however, A=Nb, and Ta and V --) currently indicated by JP,61-250905,A (Ba1-x Srx O) It is Baalphacalcium1-alphaSiO3 of a vitreous state to the barium titanate currently indicated by L=Y or rare earth elements, and JP,2-83256,A. What was added is mentioned. However, neither of these dielectric porcelain constituents was able to have the good temperature characteristic of capacity, there could not be little aging of the capacity under direct-current electric field, and all the properties that accelerated aging of insulation resistance is long were not able to be satisfied. For example, accelerated aging of insulation resistance is short what is indicated by JP,61-250905,A and JP,2-83256,A, respectively.
[0010]
[Problem(s) to be Solved by the Invention] As for this invention, accelerated aging of insulation resistance IR aims [aging of the capacity under direct-current electric field] are made from such a situation, and can satisfy each X7R property (EIA standard) and the B weighting (EIAJ standards) which are the temperature characteristic of capacity, and small at offering a long laminating type ceramic chip capacitor.
[0011]
[Means for Solving the Problem] Such a purpose is attained by this invention of following the (1) - (7).
It is the laminating type ceramic chip capacitor which has the capacitor chip object of composition of that the laminating of a dielectric layer and the internal-electrode layer was carried out by turns. the aforementioned dielectric layer a barium titanate as an accessory constituent as a principal component (1) A magnesium oxide, Manganese oxide and at least one sort chosen from a barium oxide and a calcium oxide, Silicon oxide is contained and it is a barium titanate BaTiO3 A magnesium oxide to MgO manganese oxide -- MnO -- a barium oxide -- BaO -- a calcium oxide -- CaO -- silicon oxide -- SiO2 When it converts,

respectively The ratio to 3100 mol of BaTiO(s) is MgO:0.1-3 mol, MnO:0.05-1.0 mol, BaO+CaO:2-12 mol, and SiO2. : Laminating type ceramic chip capacitor characterized by being 2-12 mols.
(2) It is BaO, CaO, and SiO2 to the above BaTiO3 and the sum total of MgO and MnO. Laminating type ceramic chip capacitor of the above (1) contained one to 10% of the weight as y (Bax calcium1-x O) and SiO2 (however, it is 0.3<=x<=0.7 and 0.95<=y<=1.05.).
It is the laminating type ceramic chip capacitor which has the capacitor chip object of composition of that the laminating of a dielectric layer and the internal-electrode layer was carried out by turns. the aforementioned dielectric layer a barium titanate as an accessory constituent as a principal component (3) A magnesium oxide, Manganese oxide, a yttrium oxide, and at least one sort chosen from a barium oxide and a calcium oxide, Silicon oxide is contained and it is a barium titanate BaTiO3 A magnesium oxide to MgO To MnO, it is a yttrium oxide about manganese oxide Y2 O3 In BaO, it is [barium oxide] silicon oxide to CaO about a calcium oxide SiO2 When it converts, respectively, The ratio to BaTiO3 100 mol is MgO:0.1-3 mol, MnO:0.05-1.0 mol, and Y2 O3. : One mol or less, BaO+CaO:2-12 mol, SiO2 : Laminating type ceramic chip capacitor characterized by being 2-12 mols.
(4) BaTiO3, MgO, MnO, and Y2 O3 It is BaO, CaO, and SiO2 to the sum total. Laminating type ceramic chip capacitor of the above (3) contained one to 10% of the weight as y (Bax calcium1-x O) and SiO2 (however, it is 0.3<=x<=0.7 and 0.95<=y<=1.05.).
(5) The above (1) whose electric conduction material contained in the aforementioned internal-electrode layer is nickel or nickel alloy, or one laminating type ceramic chip capacitor of (4).
(6) Oxygen tension is 10-8 to 10-12. Laminating type ceramic chip capacitor of the above (5) calcinated within the 1200-1400-degree C temperature requirement in the atmosphere which is atmospheric pressure.
(7) The above (5) or (6) laminating type ceramic chip capacitors which annealed oxygen tension within the temperature requirement 1100 degrees C or less in the atmosphere of 10 to 6 or more atmospheric pressure after baking.
[0012]
[Elements of the Invention] Hereafter, the concrete composition of this invention is explained in detail.
[0013] The cross section of the example of composition of the laminating type ceramic chip capacitor of a [laminating type ceramic chip-capacitor] this invention is shown in drawing 1 .
[0014] As shown in drawing 1 , the laminating type ceramic chip capacitor 1 of this invention has the capacitor chip object 10 of composition of that the laminating of a dielectric layer 2 and the internal-electrode layer 3 was carried out by turns, and has the internal-electrode layer 3 and the flowing external electrode 4 on this capacitor chip object 10 front face. Although there is especially no limit in the configuration of the capacitor chip object 10, it usually considers as the shape of a rectangular parallelepiped. Moreover, although what is necessary is for there to be especially no limit also in the size, and just to consider as a suitable size according to a use, it is usually x(1.0-5.6mm) (0.5-5.0mm) x (0.5-1.9mm) grade. The laminating of the internal-electrode layer 3 is carried out so that the end face may be exposed to two front faces on which the capacitor chip object 10 counters by turns, the external electrode 4 is formed in the two aforementioned front faces of the capacitor chip object 10 which carry out opposite, and it constitutes a predetermined capacitor circuit.
[0015] The <dielectric-layer 2> dielectric layer 2 contains a magnesium oxide, manganese oxide, at least one sort chosen from a barium oxide and a calcium oxide, and silicon oxide as a barium titanate and an accessory constituent as a principal component. a barium titanate -- BaTiO3 a magnesium oxide -- MgO -- manganese oxide -- MnO -- a barium oxide -- BaO -- a calcium oxide -- CaO -- silicon oxide -- SiO2 When it converts, respectively The ratio of each compound in a dielectric layer receives BaTiO3 100 mol. MgO:0.1-3 mol, desirable -- 0.5-1.5 mols and MnO:0.05-1.0 mol -- desirable -- 0.2-0.4 mols, BaO+CaO:2-12 mol, and SiO2 : It is 2-12 mols.
[0016] (BaO+CaO) /SiO2 Although not limited especially, being referred to as 0.9-1.1 is usually desirable. BaO, CaO, and SiO2 y (Bax calcium1-x O) and SiO2 It may be contained by carrying out. In this case, in order to obtain a precise sintered compact, it is desirable to be referred to as 0.3<=x<=0.7 and 0.95<=y<=1.05. (Bax calcium1-x O) y and SiO2 A content is 4 - 6 % of the weight more preferably one to 10% of the weight to the sum total of BaTiO3, and MgO and MnO. In addition, the content of the metallic element which especially the oxidation state of each oxide is not limited, but constitutes each oxide should just be the above-mentioned range.
[0017] In a dielectric layer 2, it is BaTiO3. It is Y2 O3 to 100 mols of converted barium titanates. It is desirable that convert and a yttrium oxide one mol or less is contained as an accessory constituent. Y2 O3 Although there is especially no minimum of a content, in order to realize sufficient effect, it is desirable that 0.1 mols or more are contained. When a yttrium oxide is included, they are y (Bax calcium1-x O) and SiO2. A content is BaTiO3, MgO, MnO, and Y2 O3. It is 4 - 6 % of the weight more preferably one to 10% of the weight to the sum total.
[0018] In addition, although other compounds may be contained in the dielectric layer 2, since cobalt oxide increases capacity rate of change, not being contained substantially is desirable [cobalt oxide].
[0019] The reason for limitation of the content of each above-mentioned accessory constituent is as follows.
[0020] It cannot consider as the range of the request of the temperature characteristic of capacity by the content of a magnesium oxide being under the aforementioned range. If the content of a magnesium oxide exceeds the aforementioned range, a degree of sintering gets worse rapidly, precise-izing will become inadequate, and IR accelerated aging will fall, and high specific inductive capacity will not be obtained.
[0021] Good reducing one-proof is not obtained as the content of manganese oxide is under the aforementioned range, but IR accelerated aging becomes inadequate, and it loses. It becomes difficult to make tandelta low. When the content of manganese

oxide is over the aforementioned range, it becomes difficult to make small aging of the capacity at the time of direct-current electric-field impression.
[0022] BaO+CaO, and y (Bax calcium1-x O) and SiO2 If there are too few contents, aging of the capacity at the time of direct-current electric-field impression will become large, and IR accelerated aging will become inadequate. [SiO2 and] If there are too many contents, the rapid decline in specific inductive capacity will take place.
[0023] A yttrium oxide has the effect which raises IR accelerated aging. When the content of a yttrium oxide exceeds the aforementioned range, electrostatic capacity decreases, and a degree of sintering falls, and there is a bird clapper that precise-izing is inadequate.
[0024] Moreover, the aluminum oxide may contain in the dielectric layer. An aluminum oxide has the operation which enables sintering at low temperature comparatively. aluminum 2O3 As for the content of the aluminum oxide when converting, it is desirable to carry out to 1 or less % of the weight of the whole dielectric materials. If there are too many contents of an aluminum oxide, the problem of checking sintering conversely will be produced.
[0025] In this invention, the dielectric layer has the so-called core-shell structure. That is, it has the structure where the grain boundary (shell) of a low dielectric constant phase encloses the circumference of the crystal grain (core) of a high dielectric constant phase. BaO, TiO2, MnO, CaO, etc. usually contain in a core -- having -- shell -- usually -- CaO, TiO2, BaO, SiO2, MnO, MgO, and Y2 O3 etc. -- it is contained
[0026] By considering as the above-mentioned composition, although especially the diameter of average crystal grain of a dielectric layer is not limited, detailed crystal grain is obtained and the diameter of average crystal grain is usually 0.2-0.7 micrometers. It becomes a grade. Moreover, the average width of face of shell is 0.02-0.2 micrometers. It is a grade.
[0027] Although the Curie temperature of a dielectric layer can be suitably set up by choosing composition according to the specification applied, generally it usually makes 85 degrees C or more about 120-135 degrees C.
[0028] The thickness of a dielectric layer which is a hit much more is 100 micrometers. It is especially 50 micrometers hereafter. The following and further 2-20 micrometers It considers as a grade. this invention is effective in aging prevention of the capacity of the laminating type ceramic chip capacitor which has such a thin-layer-ized dielectric layer. In addition, the number of laminatings of a dielectric layer is usually made about into two to 200.
[0029] Although especially the electric conduction material contained in the <internal-electrode layer 3> internal-electrode layer 3 is not limited, since dielectric-layer 2 component has reducing one-proof, base metal can be used. As a base metal used as electric conduction material, nickel or nickel alloy is desirable. As a nickel alloy, the alloy of one or more sorts of elements and nickel which are chosen from Mn, Cr, Co, and aluminum is desirable, and, as for nickel content in an alloy, it is desirable that it is 95 % of the weight or more.
[0030] In addition, in nickel or nickel alloy, various minor constituents, such as P, may be contained about 0.1 or less % of the weight.
[0031] Internal-electrode layer thickness is usually 1-5 micrometers, although what is necessary is to just be suitably determined according to a use etc. It is 2-3 micrometers especially. It is desirable that it is a grade.
[0032] Although especially the electric conduction material contained in the <external electrode 4> external electrode 4 is not limited, cheap nickel, Cu(s), and these alloys can be used in this invention.
[0033] The thickness of an external electrode is usually 10-50 micrometers, although what is necessary is to just be suitably determined according to a use etc. It is desirable that it is a grade.
[0034] The laminating type ceramic chip capacitor of the [manufacture method of laminating type ceramic chip capacitor] this invention is manufactured by printing or imprinting and calcinating an external electrode, after producing a green chip by usual print processes and the usual sheet method for having used the paste and calcinating this.
[0035] The paste for <paste for dielectric layers> dielectric layers kneads a dielectric raw material and an organic vehicle, and is manufactured.
[0036] Although the mixture of the above-mentioned multiple oxide and the above-mentioned oxide can be used for a dielectric raw material, it can choose from the various compounds used as the multiple oxide described above by baking, or an oxide, for example, a carbonate, an oxalate, a nitrate, a hydroxide, an organometallic compound, etc. suitably, it can mix, and can use. What is necessary is just to determine that the content of each compound in a dielectric raw material will serve as composition of a dielectric layer described above after baking.
[0037] A dielectric raw material is usually 0.1-1 micrometer of mean particle diameters. It is used as powder of a grade.
[0038] With an organic vehicle, a binder is dissolved into the organic solvent. What is necessary is not to limit especially the binder used for an organic vehicle, but just to choose it from the various usual binders, such as an ethyl cellulose, suitably. Moreover, what is necessary is not to limit especially the organic solvent to be used, either but just to choose print processes, the sheet method, etc. from various organic solvents, such as a terpineol, a butyl carbitol, an acetone, and toluene, suitably according to the method of using.
[0039] The paste for <paste for internal-electrode layers> internal-electrode layers kneads and prepares the various oxides used as the electric conduction material which consists of the various above-mentioned conductive metals or an alloy, or the electric conduction material described above after baking, an organometallic compound, resinate, etc. and the above-mentioned organic vehicle.
[0040] What is necessary is just to prepare the paste for <paste for external electrodes> external electrodes like the above-mentioned paste for internal-electrode layers.
[0041] <Organic vehicle content> What is necessary is for there to be especially no limit in the content of the organic vehicle

under each above-mentioned paste, and to make the usual content, for example, a binder, and just to make a solvent into about 10 - 50 % of the weight about 1 to 5% of the weight. Moreover, during each paste, the additive chosen from various dispersants, a plasticizer, a dielectric, an insulator, etc. if needed may contain. As for these total contents, it is desirable to consider as 10 or less % of the weight.

[0042] When using <green chip production> print processes, after carrying out laminating printing on substrates, such as PET, and cutting the paste for dielectric layers, and the paste for internal-electrode layers in a predetermined configuration, it exfoliates from a substrate and they are considered as a green chip.

[0043] Moreover, when using the sheet method, after forming a green sheet using the paste for dielectric layers and printing the paste for internal-electrode layers on this, the laminating of these is carried out and it considers as a green chip.

[0044] Although what is necessary is just to perform ** binder processing performed before <** binder processing> baking on condition that usual, when using base metal, such as nickel and nickel alloy, for the electric conduction material of an internal-electrode layer, it is desirable to carry out on condition that the following especially.

programming-rate: -- 5-300 degrees C/hour -- especially -- 10-100 degree-C/hour retention-temperature:200-400 degree C -- especially -- 250-300-degree-C temperature holding-time:0.5 - 24 hours -- especially -- the inside of 5 - 20-hour atmosphere:air -- [0045] Although the atmosphere at the time of <baking> green chip baking should just be suitably determined according to the kind of electric conduction material under paste for internal-electrode layers, when using base metal, such as nickel and nickel alloy, as electric conduction material, the oxygen tension in a firing environments is 10-8 to 10-12. Considering as atmospheric pressure is desirable. The electric conduction material of an internal-electrode layer causes unusual sintering as oxygen tension is under the aforementioned range, and there is way piece **********. Moreover, when oxygen tension exceeds the aforementioned range, it is in the inclination for an internal-electrode layer to oxidize.

[0046] Moreover, as for especially the retention temperature at the time of baking, it is desirable to consider as 1250-1300 degrees C 1200-1400 degrees C. If precise-izing is inadequate in a retention temperature being under the aforementioned range and the aforementioned range is exceeded, aging of the capacity at the time of direct-current electric-field impression will become large.

[0047] As for various conditions other than the above-mentioned condition, it is desirable to perform it as follows.

programming-rate: -- 50-500 degrees C/hour -- especially -- 200-300-degree-C [/] hour temperature holding-time:0.5 - 8 hours -- especially -- 1 - 3-hour cooling rate: -- especially 200-300-degree-C [/] firing environments makes a reducing atmosphere 50-500 degrees C /an hour an hour -- desirable -- as a controlled atmosphere -- N2 H2 It is desirable to humidify and use mixed gas.

[0048] When it calcinates in a <annealing> reducing atmosphere, it is desirable that annealing is given to a capacitor chip object. Annealing is processing for reoxidating a dielectric layer, and, thereby, can lengthen IR accelerated aging remarkable.

[0049] As for especially the oxygen tension in annealing atmosphere, it is desirable to consider as 10-5 - 10-4 atmospheric pressure 10 to 6 or more atmospheric pressure. When reoxidation of a dielectric layer is difficult in oxygen tension being under the aforementioned range and the aforementioned range is exceeded, it is in the inclination for an internal-electrode layer to oxidize.

[0050] As for especially the retention temperature in the case of annealing, it is desirable to consider as 500-1000 degrees C 1100 degrees C or less. It is in the inclination for oxidizing [of a dielectric layer] to become that a retention temperature is under the aforementioned range inadequate, and for a life to become short, and if the aforementioned range is exceeded, an internal-electrode layer will oxidize, and it reacts with the dielectric voxel ground and capacity not only falls, but is in the inclination for a life to also become short. In addition, annealing may consist of only a temperature up and a temperature fall. In this case, the temperature holding time is zero and retention temperatures are a maximum temperature and homonymy.

[0051] As for various conditions other than the above-mentioned condition, it is desirable to perform it as follows.

temperature holding-time: -- 0 - 20 hours -- especially -- 6 - 10-hour cooling rate: -- N2 especially humidified in the gas for 100-300-degree-C [/] atmosphere an hour an hour 50-500 degrees C /It is desirable to use gas etc.

[0052] In addition, it sets to ** binder processing, above-mentioned baking, and above-mentioned annealing, and is N2. What is necessary is just to use WETTA etc., in order to humidify gas, mixed gas, etc. In this case, about 5-75 degrees C of water temperature are desirable.

[0053] Even if it carries out continuously, you may perform ** binder processing, baking, and annealing independently.

[0054] When these are performed continuously, it calcinates by having changed [without cooling] atmosphere and carried out the temperature up to the retention temperature in the case of baking continuously, it subsequently cools and the retention temperature of annealing is reached after ** binder processing, it is desirable to change atmosphere and to perform annealing.

[0055] Moreover, when performing these independently, baking is faced, and it is N2 to the retention temperature at the time of ** binder processing. Gas or N2 humidified After it is desirable to change atmosphere and to continue a temperature up further, after carrying out a temperature up under gas atmosphere and it cools to the retention temperature at the time of annealing, it is N2 again. Gas or N2 humidified It is desirable to change into gas atmosphere and to continue cooling. Moreover, annealing is faced and it is N2. N2 which could change atmosphere and humidified all the processes of annealing after carrying out a temperature up to a retention temperature under gas atmosphere It is good also as a gas atmosphere.

[0056] <External electrode formation> End-face polish is given with barrel finishing, sandblasting, etc., it prints or imprints on the capacitor chip object acquired as mentioned above, the paste for external electrodes is calcinated on it, and the external electrode 4 is formed. As for the baking conditions of the paste for external electrodes, it is desirable to consider as for [10 minutes] - about 1 hour at 600-800 degrees C.

[0057] And an enveloping layer is formed in external electrode 4 front face with plating etc. if needed.
[0058] Thus, the laminating type ceramic chip capacitor of the manufactured this invention is mounted on a printed circuit board etc. with a pewter etc., and is used for various electronic equipment etc.
[0059] And in the dielectric layer of the laminating type ceramic chip capacitor of this invention, it is 0.02v/micrometer at the time of use. Above It is 0.2v/micrometer especially. It is 0.5 morev/micrometer above. Generally it is 5v/micrometer above. Although the direct-current electric field below a grade and the alternating current component usually superimposed on this are impressed, even if it carries out the load of such direct-current electric field, there is very little aging of capacity.
[0060]
[Example] Hereafter, the concrete example of this invention is given and this invention is further explained to a detail.
[0061] Each following paste was prepared.
paste particle size for dielectric layers of 0.1-1 micrometer BaTiO3, 4 (MgCO3), Mg(OH)2 and 5H2 O, MnCO3, SiO (Ba0.5 calcium0.5)3, and Y2 O3 from -- wet blending of the selected material powder was carried out with the ball mill for 16 hours, and subsequently it was made to dry by the spray dryer, and considered as the dielectric raw material The mixed ratio of each powder was changed and two or more dielectric raw materials were produced.
[0062] Each dielectric raw material 100 weight section, and the acrylic resin 4.8 weight section, the methylene-chloride 40 weight section, the trichloroethane 20 weight section, the mineral spirit 6 weight section and the acetone 4 weight section were mixed and pasted with the ball mill.
[0063] 0.8 micrometers of paste mean particle diameters for internal-electrode layers The nickel particle 100 weight section, and the organic vehicle (what dissolved the ethyl-cellulose resin 8 weight section in the butyl carbitol 92 weight section) 40 weight section and the butyl carbitol 10 weight section were kneaded with 3 rolls, and were pasted.
[0064] 0.5 micrometers of paste mean particle diameters for external electrodes The Cu particle 100 weight section, and the organic vehicle (what dissolved the ethyl-cellulose resin 8 weight section in the butyl carbitol 92 weight section) 35 weight section and the butyl carbitol 7 weight section were kneaded and pasted.
[0065] The laminating type ceramic condenser of composition of being shown in drawing 1 was produced using each above-mentioned paste for dielectric layers, and the above-mentioned paste for internal-electrode layers.
[0066] First, the green sheet was produced on the PET film using the paste for dielectric layers, and the paste for internal-electrode layers was printed on this. Subsequently, from the PET film, it exfoliated and the laminating of the sheet was carried out, pressurization adhesion was carried out and the green chip was obtained. The number of laminatings was made into four layers.
[0067] Subsequently, the green chip was cut in predetermined size, ** binder processing, baking, and annealing were continuously performed on condition that the following, and the capacitor chip object was produced.
[0068] ** binder processing programming-rate: -- 15-degree-C [/] hour retention-temperature: -- 280-degree-C temperature holding-time: -- 8-hour controlled-atmosphere: -- the inside of air -- [0069] baking programming-rate: -- 200-degree-C [/] hour retention-temperature: -- 1300-degree-C temperature holding-time: -- 2-hour cooling rate: -- 300-degree-C [/] hour controlled-atmosphere: -- N2 humidified H2 mixed-gas oxygen tension: -- 10-9 atmospheric pressure [0070] annealing retention-temperature: -- 900-degree-C temperature holding-time: -- 9-hour cooling rate: -- 300-degree-C [/] hour controlled-atmosphere: -- N2 humidified gas oxygen tension: -- 10-5 atmospheric pressure [0071] In addition, water temperature was made into 35 degrees C at humidification of each controlled atmosphere using WETTA.
[0072] After grinding the end face of the acquired capacitor chip object with sandblasting, the above-mentioned paste for external electrodes is imprinted to the aforementioned end face, and it is N2+H2. It calcinated for 10 minutes at 800 degrees C in atmosphere, the external electrode was formed, and the laminating type ceramic chip-capacitor sample was obtained.
[0073] thus, the size of each manufactured sample -- 3.2mmx1.6mmx1.2mm -- it is -- the thickness of a dielectric layer -- 15 micrometers internal-electrode layer thickness -- 2.5 micrometers it was .
[0074] Composition of the dielectric layer of each sample is shown in the following table 1. These composition was computed in accordance with the criteria mentioned above. SiO(Ba, calcium) 3 [in addition,] in Table 1 SiO (Ba0.5 calcium0.5)3 it is .
[0075] The following measurement was performed about each sample. A result is shown in Table 1.
[0076] The temperature-characteristic X7R property of capacity: By the LCR meter, it is measurement voltage 1V about -55-125 degrees C. Capacity was measured and it investigated whether capacity rate of change would satisfy less than (25 degrees C of reference temperature) **15%. The case of being satisfied was made as O and the case of not being satisfied was made into x.
[0077] 1 micrometer in thickness of the aging dielectric layer of the capacity under direct-current electric field Hit 1.06V Direct-current electric field (applied-voltage 16V to a sample) are impressed at 40 degrees C for 66 hours, subsequently, after leaving it at a room temperature in unladen for 24 hours, capacity is measured and it asks for variation deltaC from the capacity C0 before direct-current electric-field impression (initial capacity), and it is rate-of-change deltaC/C0. It computed. In addition, capacity was measured on the above-mentioned conditions.
[0078] It is 10v/micrometer in 180 degrees C of accelerated aging of insulation resistance IR. An accelerated test is performed under electric field and resistance (IR) is 2x105. Time until it becomes below omega was made into the lifetime.
[0079] The specific inductive capacity in the specific inductive capacity of epsilons25 degrees C was measured.
[0080]
[Table 1]

サンプル No.	誘電体層組成 MgO (モル)	MnO (モル)	(Ba,Ca)SiO$_3$ (wt%)	Y_2O_3 (モル)	温度特性 X7R	ΔC/C$_0$ (%)	IR加速寿命 (時間)	ε_s (25 ℃)
1	1	0.375	5	0	○	-1.42	2.7	2871
2	1	0.375	5	0.04	○	-1.58	5.0	2729
3	1	0.375	5	0.09	○	-1.23	11.3	2565
4	1	0.375	5	0.18	○	-1.58	13.9	2495
5	1	0.375	5	0.27	○	-1.85	27.3	2530
6	1	0.19	5	0	○	-0.65	5.0	2758
7	1	0.19	5	0.04	○	-0.85	5.2	2663
8	1	0.19	5	0.09	○	-1.13	4.2	2670
9	1	0.19	5	0.18	○	-0.43	9.7	2760
10	1	0.19	5	0.27	○	-0.16	14.9	2652
11	1.2	0.375	5	0	○	-0.06	2.2	2952
12	1.2	0.375	5	0.04	○	-0.25	7.6	2772
13	1.2	0.375	5	0.09	○	-0.71	6.0	2895
14	1.2	0.375	5	0.18	○	-2.44	15.3	2542
15	1.2	0.375	5	0.27	○	-2.75	34.3	2359
16 (比較)	0*	0.1	5	0.2	×	-5.11	1.0	5241
17 (比較)	1	0*	5	0.2	×	-0.52	0.1	3218
18 (比較)	1	2*	5	0.2	○	-5.77	5.4	2153
19 (比較)	1	0.1	0*	0.2	×	-8.38	0	4827

＊：本発明範囲を外れる組成

[0081] From the result shown in Table 1 to a book That is, with the sample whose composition of a dielectric layer is within the limits of this invention, X7R property is satisfied, the rate of aging of the capacity under direct-current electric field is very as low as 10% or less, and the life of the insulation resistance IR in an accelerated test is long. And Y2 O3 Addition shows that IR accelerated aging improves remarkably. Moreover, as for this invention sample of Table 1, the temperature characteristic of electrostatic capacity was satisfied [with B weighting [-25-85 degree C] of less than (20 degrees C of reference temperature) **10% [of capacity rate of change]].

[0082] The scanning-electron-microscope photograph of the dielectric-layer cross section of sample No.16 of sample No.1 and the example of comparison of this invention is shown in drawing 2 and drawing 3 , respectively. These photographs carried out mirror polishing of the cross section, and after they **********ed with the mixed-water solution of a fluoric acid-nitric acid, they photoed it. sample No.16 (drawing 3) which are an example of comparison -- the diameter of average crystal grain -- about 1 micrometer the average width of face of the grain boundary -- about 0.2 micrometers it is -- although -- sample No.1 (drawing 2) of this invention -- the diameter of average crystal grain -- about 0.5 micrometers the average width of face of the grain boundary -- about 0.2 micrometers It is fine. In addition, the same relation was found about other comparison samples and this invention samples which are shown in Table 1.

[0083] Moreover, the transmission-electron-microscope photograph of the dielectric layer of sample No.16 of the example of comparison was taken before the above-mentioned direct-current electric-field impression and after impression. The photograph before impression is shown in drawing 4 , and the photograph after impression is shown in drawing 5 , respectively. Drawing 4 and drawing 5 show that domains are decreasing in number by impression of direct-current electric field.

[0084]

[Effect of the Invention] It can be satisfied [with this invention] of X7R property and the B weighting about the temperature characteristic of capacity by considering a dielectric layer as predetermined composition, and accelerated aging of insulation resistance IR can realize a long laminating type ceramic chip capacitor small [aging of the capacity under direct-current electric

field].

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

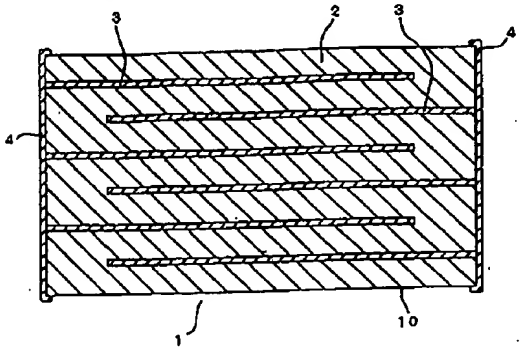
[Brief Description of the Drawings]
[Drawing 1] It is the cross section showing the example of composition of the laminating type ceramic chip capacitor of this invention.
[Drawing 2] It is the drawing substitution photograph in which a particulate structure is shown, and is the scanning-electron-microscope photograph of the dielectric-layer cross section of the laminating type ceramic chip capacitor of this invention.
[Drawing 3] It is the drawing substitution photograph in which a particulate structure is shown, and is the scanning-electron-microscope photograph of the dielectric-layer cross section of the conventional laminating type ceramic chip capacitor.
[Drawing 4] It is the drawing substitution photograph in which a particulate structure is shown, and is the transmission-electron-microscope photograph of the dielectric layer of a laminating type ceramic chip capacitor.
[Drawing 5] It is the drawing substitution photograph in which a particulate structure is shown, and is the transmission-electron-microscope photograph of the dielectric layer of the laminating type ceramic chip capacitor after direct-current electric-field impression.
[Description of Notations]
1 Laminating Type Ceramic Chip Capacitor
10 Capacitor Chip Object
2 Dielectric Layer
3 Internal-Electrode Layer
4 External Electrode

[Translation done.]

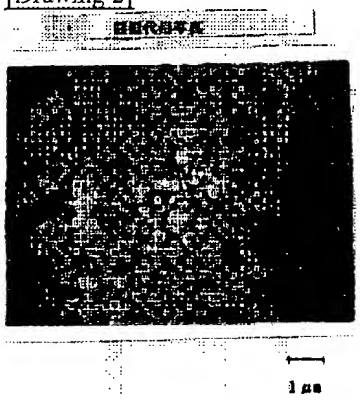
* NOTICES *

DRAWINGS

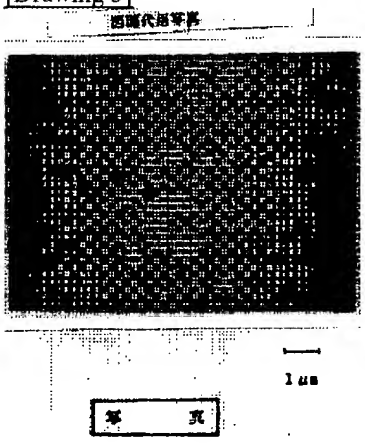
[Drawing 1]



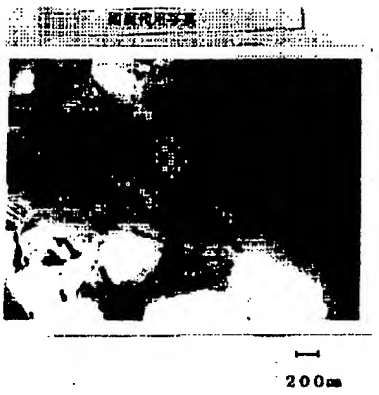
[Drawing 2]



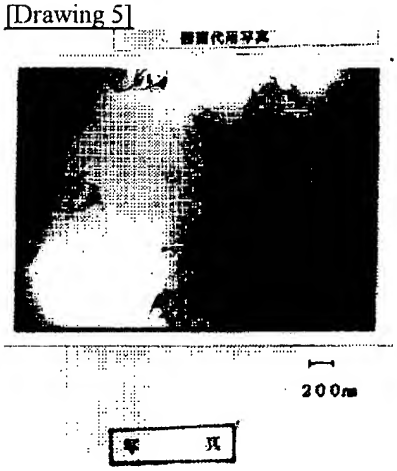
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]